Application Note - XRT73L00 DS3/E3/STS-1 LIU IC Power Conditioning Requirements

October 24, 2001

Revision 1.06

XRT73L00 DS3/E3/STS-1 LIU Power Conditioning Requirements

1.0 OVERVIEW

XRT73L00 is a combination DS3/E3/STS-1 Transceiver (Line Interface Unit) that is designed for use in multi-standard Networking and Transmission Systems.

The XRT73L00 device is a mixed signal device that supports the transmission and reception of data at the DS3, E3 and STS-1 rates. Hence, this chip handles both digital input and output signals (which switch at very fast rate and generate a lot of electrical and radio frequency noise). Additionally, this chip also consists of a sensitive analog receiver. As a consequence, the user must be careful in how to handle the VDD and GND pins, in order to ensure good performance of the XRT73L00 device.

In particular, the user's PCB layout and handling of the VDD and GND signals must accomplish the following:

1. Provide good isolation between the Transmit and Receive signals.
2. Provide good isolation between Analog and Digital signals.

In many networking or transmission systems the source of power is a DC-DC converter, which uses a switching converter to transform -48VDC input to +3.3VDC output. The switching converter typically uses a switching frequency from 20KHz to 1MHz and the 3.3VDC power normally carries a significant amount of 'ripple' noise at this switching frequency. This ripple noise can adversely affect performance of analog circuits in the mixed signal devices (XRT73L00 and similar).

This application note presents some guidelines on how to layout and filter the VDD and GND signals that are fed to the XRT73L00 device.

2.0 XRT73L00 'GND' PINS

Tie all XRT73L00 'GND' pins (pin numbers 5,6,7,25,28,39) to the system ground plane. In case there are separate analog and digital ground planes are available, tie all 'GND' pins to the analog ground. Do not insert any impedance (an inductor or ferrite bead) between analog and digital ground pins of XRT73L00.

3.0 XRT73L00 'POWER' PINS

The XRT73L00 device has five power supply pins, pin 10 is receive analog section power supply pin. Pins 3 and 42 are the transmit analog section power supply pin, and pins 26 and 29 are digital power supplies. The receive analog power supply (pin 10) is

the most critical as it powers the clock recovery phase-lock-loop and therefore power to this pin should be as clean as possible.

It is also desirable to keep the transmit power supply noise isolated from the receive power supply. In addition if multiple XRT73L00 devices are used in a system it is further desirable to keep their power isolated (from each other) in order to minimize cross-talk.

The attached schematic (Figure 1) illustrates Exar's recommendations on how to connect the Analog and Digital VDD pins (of a single XRT73L00 device) to a 3.3V Power Supply. Exar's approach recommends the use of two-stage LC filtering.

3.1 STAGE 1 – A LARGE LC FILTER (consisting of L1 and C1)

This particular LC filter consists of a 15uH inductor and a 33uF capacitor. The purpose of this LC filter is to eliminate much of the "DC-to-DC Converter-induced" low frequency ripple, within the 3.3V power supply line, prior to being routed to any of the VDD pins of the XRT73L00 device.

NOTES ABOUT THIS LC FILTER:

1. This LC filter should be placed close to the output of the DC-to-DC Converter.
2. Only one such LC filter is needed, per board (even in multi-channel applications). However, multi-channel designs may have to use multiple instantiations of this LC filter due to large voltage drops across the inductor (due to the increased amount of current draw of multiple XRT73L00 devices and the dc resistance of the inductor), or because of the maximum operating current limit of this inductor as well.
3. This LC filter may not be necessary if the 3.3V Power Supply is already filtered elsewhere in the system.

COMPONENT SELECTION FOR L1 AND C1

The XRT73L00 device draws about 140mA of current. We recommend that the user select a High Current Inductor, that has a small enough DC resistance such that the voltage drop across the inductor will not exceed 50mV. Therefore, the user should select a 15uH Inductor that has a DC resistance of less than 0.36Ω.

An example of an acceptable inductor for L1 is the 4922-15L from API-Delevan. This particular inductor has a maximum dc resistance of 0.089Ω, and has a maximum current rating of 2.11A. Contact information for API-Delevan is presented in Appendix A, at the end of this Applications Note.

The capacitor, C1, should be a 33uF 10V Tantalum capacitor, which is supplied by various manufacturers. Digikey PCT2336CT-ND or equivalent would be acceptable.

3.2 STAGE 2 – SMALLER LC FILTERING FOR RECEIVE AND TRANSMIT ANALOG VDD PINS

After the Power Supply signal passes through the large LC filter (consisting of L1 and C1), is should then be routed to three different points, in parallel.

- Directly to the Digital VDD pins of the XRT73L00 device.
- To an LC filter (consisting of L2, a 6.8µH inductor and C2, a 2.2µF capacitor), prior to being routed to the Receive Analog VDD pin (pin 10).
- To an LC filter (consisting of L3, a 6.8µH inductor and C3, a 2.2µF), prior to being routed to the Transmit Analog VDD pin (pin 42).

The purpose of this LC filter is two-fold:

1. To provide some isolation and filtering between the Digital VDD line and the Analog VDD lines.
2. To provide some isolation (and reduce cross-talk) between the Transmit and Receive Analog VDD lines.

NOTE: In contrast to the LC filter (consisting of Inductor L1 and Capacitor C1), these LC filters must not be shared with other LIU Devices.

COMPONENT SELECTION FOR L2/L3 AND C2/C3

As mentioned above, the LC filter (consisting of L2 and C2) is used to filter and isolate the power supply line, going to the Receive Analog VDD pin (pin 10). Likewise, the LC filter (consisting of L3 and C3) is used to filter and isolate the power supply line, going to the Transmit Analog VDD pin (pins 3 and 42).

NOTE: The XRT73L00 device draws 55mA via the Transmit Analog VDD pins and 60mA via the Receive Analog VDD pin.

For inductors L2 and L3, select as large a value as the selected size (0805, 1210 or 1812 etc.) will allow while keeping the DC resistance of each inductor to less than 2 ohms. The goal is to keep the power supply voltage (at the VDD pins of the XRT73L00 device) above 3.135 volts.

An example of an acceptable inductor would be the 1210-682J or the S1210-682K (each of size 1210) from API-Delevan. The 1210-682J inductor is spec'd to have a maximum dc resistance of 1.8ohms. Additionally, the 1210-682J inductor has a maximum current

rating of 321mA. The S1210-682K inductor is spec'd to have a maximum dc resistance of 1.5ohms. Further, the S1210-682K has a maximum current rating of 372mA.

3.3 THE ZENER DIODE

It is **strongly recommended** that a 3.6V 400mW Zener Diode be connected from +3.3V supply to power GND to suppress power supply transients in case of excessive charge injection into the Ground plane. These transients can occur while connecting the remote terminal or test equipment to the board via coaxial cable. Such transients can either expose integrated circuit devices to momentary 'reverse' polarity or excessive (7V to 10V) power supply voltages. These transients can severely impact the reliability of the XRT73L00 LIU IC. Most voltage regulators are too slow to respond to such transient conditions.

NOTE: This zener diode is also useful for suppressing peak overshoots and ringing (in the power supply line) following a rapid ramp in the power supply voltage, due to events such as "hot-swapping", etc.

An example of an acceptable 3.6V zener diode would be the 1N5914, which is available from various suppliers

3.4 DECOUPLING CAPACITORS

We strongly recommend that the user provide de-coupling capacitors for each VDD pin of the XRT73L00 device (Analog as well as Digital). The placement and routing of these decoupling capacitors must be such to minimize the trace length (and in-turn, inductance) between the capacitor and the corresponding VDD pin, and the capacitor and the corresponding via (which connects to the GND plane).

Miscellaneous Notes

The component values shown for capacitors and inductors are to be used as guidelines only. Use following guidelines for selecting components:

For decoupling capacitors use X7R for ceramic non-polar capacitors, solid-tantalum for polar capacitors. Avoid Z5U and electrolytic capacitors.

4.0 THE BNC CONNECTOR SHIELD

As a general rule, we highly recommend that the customer either AC or DC couple the BNC connector shield to Frame or Chassis Ground. In the schematic design, we recommend that the customer AC couple the BNC connectors (on both the Transmit and Receive Sides) to Frame GND. Further, we also recommend that the customer also design in a Jumper, which permits installation personnel to DC couple the BNC connector shield to Frame GND, when set.

Component selection for the for the Capacitor (used to AC couple the BNC Connector Shield to GND)
The characteristics of a capacitor, to be used in this role are as follows.

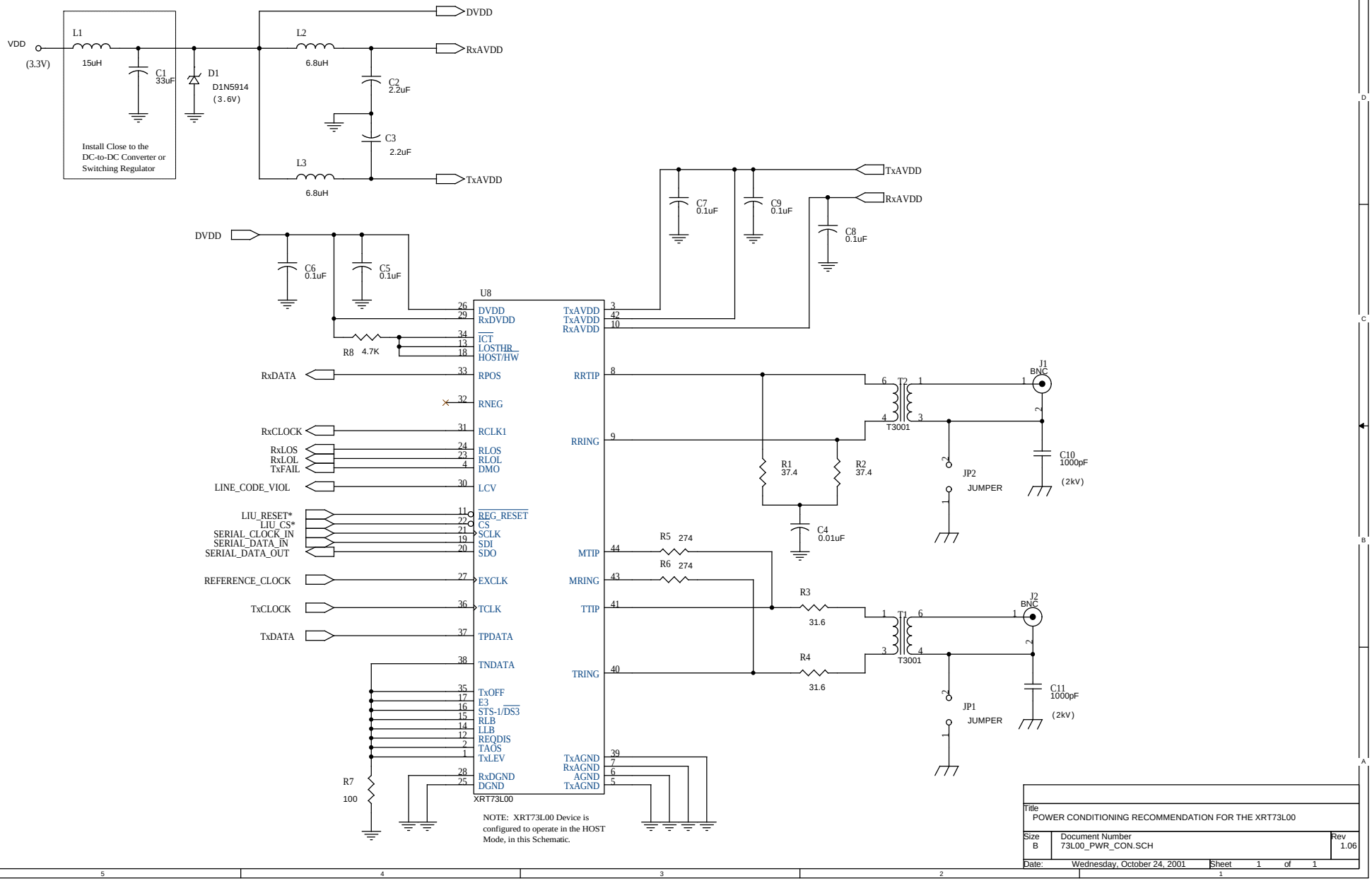
- This capacitor must be rated for high voltages.
- This capacitor must impose minimum AC impedance to Frame GND.

Therefore, the optimum choice for such a capacitor would be a capacitor that has a very high voltage rating and very large capacitance. The best capacitor that we could find that has both of these characteristics is a 1000pF capacitor that has a working voltage of 2000V.

SOME ACCEPTABLE CAPACITORS for AC Coupling the BNC Connector to Frame GND

Any of the following capacitors are suitable for this applicable. In all cases, these are Ceramic, X7R, 1000pF, 2kV, 10% capacitors which come in a 1812 case size.

Manufacturer	**Part Number**
AVX	1812GC102KA11A
AVX	1812GC102KAT2A
CALCHIP	CHV1812N2K0102KXT
JARO	CC1812XR102JN202ER
JARO	CC1812XR102KN202ER
MURATA	GRM43-2X7R102K2KVAL
JOHANSON	202S43W102KV4E



Title	POWER CONDITIONING RECOMMENDATION FOR THE XRT73L00	
Size B	Document Number 73L00_PWR_CON.SCH	Rev 1.06
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APPENDIX A

CONTACT INFORMATION FOR API-DELEVAN:

Corporate Office
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270 Quaker Road
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Phone: 716-652-3600
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APPENDIX B – CHANGES FROM PREVIOUS REVISION OF TAN-043

CHANGES FROM REVISION 1.05

Corrected schematic design. Insured that "TxAVDD" pins are connected to the "TxAVDD" power supply line. Also insured that the "RxAVDD" pin is connected to the "RxAVDD" power supply line.

CHANGES FROM REVISION 1.04

Included a list of acceptable part numbers for capacitors that can be used to AC couple the BNC Connector shield to Frame GND (Section 4.0).

CHANGES FROM REVISION 1.03

Added Section 4.0 "THE BNC CONNECTOR SHIELD" to this Ap Note.

CHANGES FROM REVISION 1.02

Update Schematic to include Jumpers JP1 and JP2, and Capacitors C10 and C11. These changes were included in order to permit System Installation personnel to either AC or DC couple the BNC connector to Frame GND.

CHANGES FROM REVISION 1.01

Updated Text, on Page 4, to reflect the recommendation of the use of the 1N5914 3.6V zener diode.

CHANGES FROM REVISION 1.00

Modified Schematic to reflect the following.

a. BNC Connector shield (on Receive Side) should be either AC or DC coupled to Frame Ground.
b. BNC Connector shield (on Receive Side) should be either AC or DC coupled to Frame Ground.
c. L1 should be changed to a 15µH inductor.
d. C1 should be changed to a 33µH inductor.
e. Specific recommendations were made to the following inductors:
    i. 1210-682J (from API-Delevan)
    ii. 4922-15L (from API-Delevan).